



Virtualization technologies: design and implementation

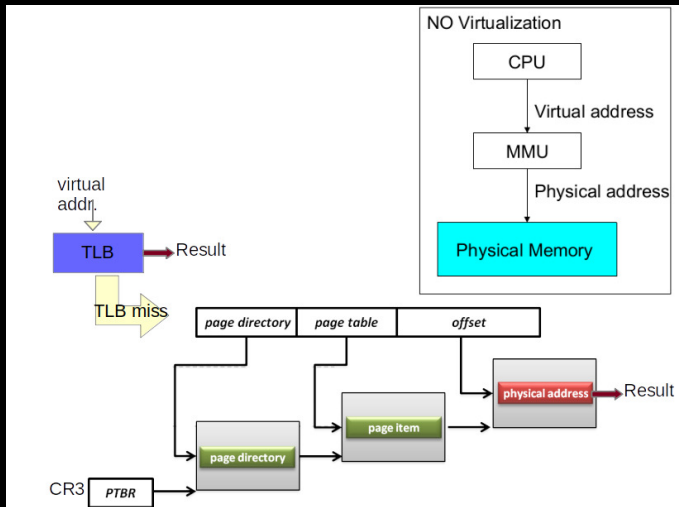
Alain Tchana - (alain.tchana@grenoble-inp.fr)

krakOS - France

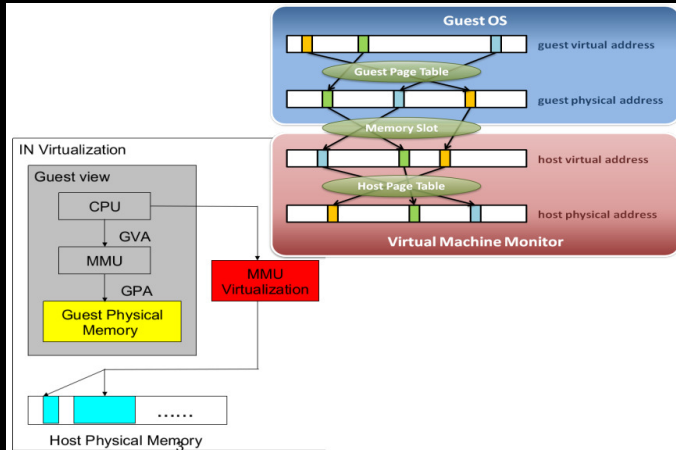
1 Memory virtualization

- 2 Project Out of Hypervisor (OoH)
 - Memory page access tracking
 - VM migration lab

Memory virtualization



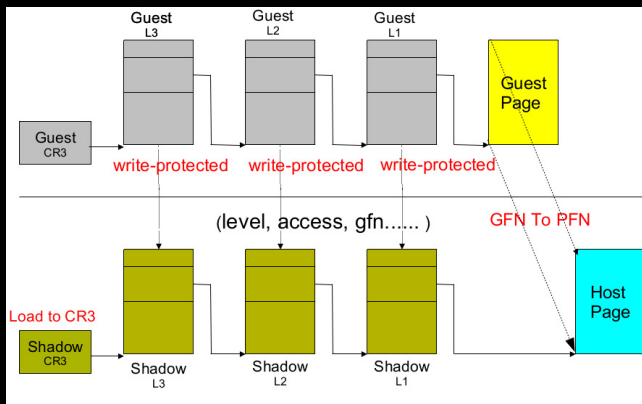
Memory virtualization



► GVA, GPA, HPA

Memory virtualization

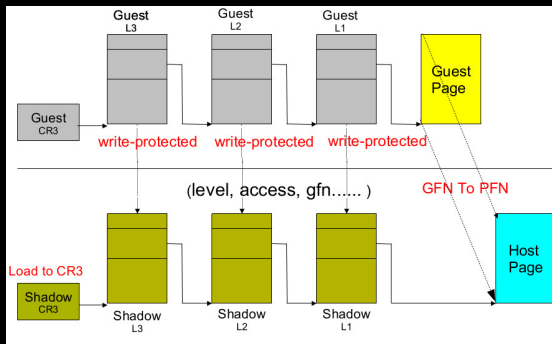
Soft MMU virtualization: Shadow paging



Memory virtualization

Soft MMU virtualization: Shadow paging

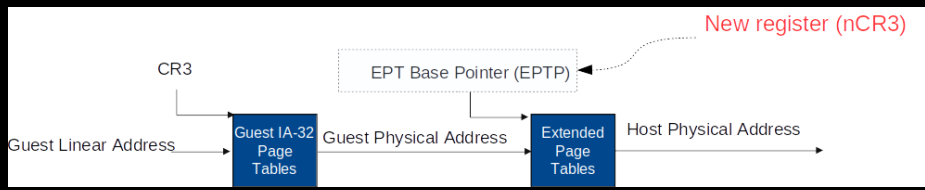
► Page table synchronization



Memory virtualization

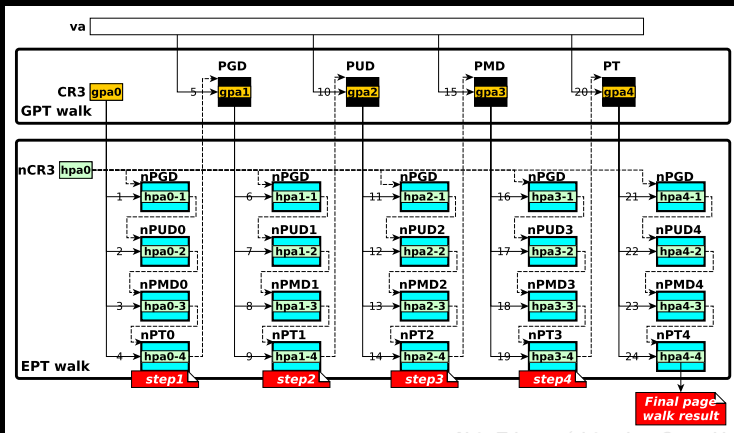
Hardware MMU virtualization: Extended (Intel)/Nested (AMD) paging

- ▶ Guest Page Table (GPT): manages by the guest
- ▶ Extended (Intel)/Nested (AMD) Page Table (EPT): manages by the hypervisor
- ▶ MMU: walks the 2 page tables at the same time



Memory virtualization

Hardware MMU virtualization: Extended (Intel)/Nested (AMD) paging

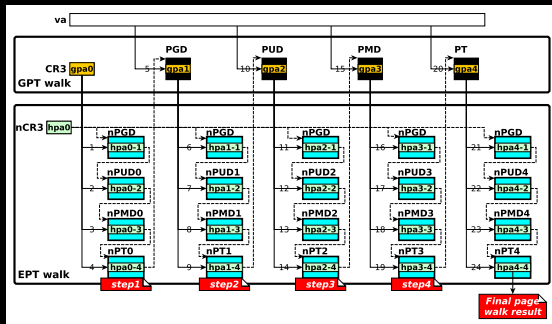


Memory virtualization

Hardware MMU virtualization: Extended (Intel)/Nested (AMD) paging

- ▶ Consequences

- ▶ 2-dimensional page table walk (24 mem. accesses on TLB miss)



Memory virtualization

Compromis

- ▶ Shadow paging
 - ▶ Advantages: 4 memory accesses on TLB miss
 - ▶ Disadvantages: Page table synchronization
- ▶ EPT
 - ▶ Advantages: no need for page table synchronization
 - ▶ Disadvantages: 2-dimensional page table walk

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Memory page access tracking

Motivations

- ▶ Live migration, checkpointing, etc.

Classical approach

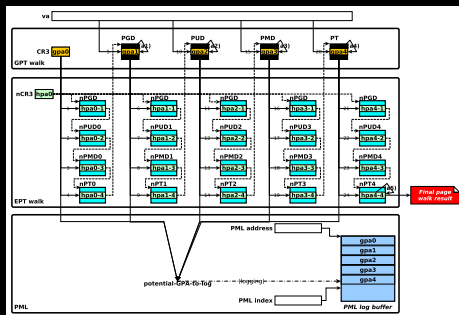
Functioning

- ▶ Write/read protect pages or Present bit invalidation
 - ▶ on access/write, fault, and trap inside the hypervisor
- ▶ Issue
 - ▶ Performance degradation due to trapping

Intel Page Modification Logging (PML)

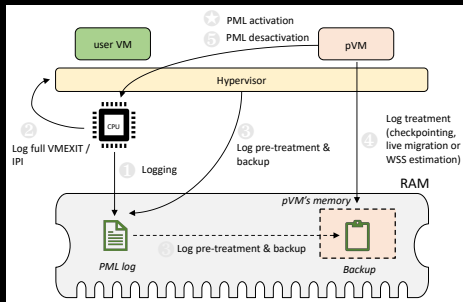
Functioning

- ▶ Invented in 2015 by Intel in collaboration with VMware
- ▶ Needs EPT
- ▶ One logging buffer per vCPU



Intel Page Modification Logging (PML)

Functioning



VM migration lab

- ▶ VM migration
 - ▶ with hap=0 and hap=1 in the VM config. file
- ▶ Check PML utilization by tracing Xen source code